(REV. 7-80)PATENT AND TRADEMARK OFFICE LIST OF PRIOR ART				Atty. Docket N . BUR920020094US1 (Serial N .			
			17 2003 - 62	Applicant Douglas D. Coolbaug	h, et al.	·		
(Use several sheets if necessary)				Filing Date	Group Unassigned			
J.S. PAT	ENT C	OCUMENTS		•		-	,	
EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS		IG DATE propriete)
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OREIGN	N PATI	ENT DOCUMENTS				·		
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
LV		JP5275619	10/22/1993	JAPAN			YES	NO
THER PI	NOR A	RT (Including Author, Ti	tle, Date, Pertine	nt Pages, Etc.)		1		
W		C.H. Lee, IBM Disclosure Bulletin "Polysilicon Resistors Compatible with Bipolar Integrated Circuits ad Method of Manufacture", Vol. 25, No. 5, October 1982; and						
W		G.R. Goth, et al., IBM Disclosure Bulletin "Planar Self-Aligned Metal/Sidewall and Polysilicon-Resistor Process", Vol. 25, No. 2, July 1982.						
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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention

PRECISION POLYSILICON RESISTOR PROCESS

Application Number :

Confirmation Number:

First Named Applicant:

Douglas Coolbaugh

Attorney Docket Number:

BUR920020094US1

Art Unit:

Examiner:

Search string:

(4256515 or 4502894 or 4604789 or 4679170 or 4929570 or 5506158 or 5554554

or 5585302 or 6184103 or 6249029 or 6255185 or 6399456 or 6400252).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
LV	1	4256515	1981-03-17	Miles et al	-		
	2	4502894	1985-03-05	Seto et al			
	3	4604789	1986-08-12	Bourassa			
	4	4679170	1987-07-07	Bourassa et al.			
	5	4929570	1990-05-29	Howell			
	6	5506158	1996-04-09	Eklund	_		
	7	5554554	1996-09-10	Bastani et al.			
	8	5585302	1996-12-17	Li			
	9	6184103	2001-02-06	Li et al.			_
	10	6249029	2001-06-19	Bryant et al.			
	11	6255185	2001-07-03	Collbaugh et al.			
	12	6399456	2002-06-04	Huang et al.			-
LV	13	6400252	2002-06-04	Smith et al.			

Signature

Examiner Name	Date
LAN VINH	5/1/05